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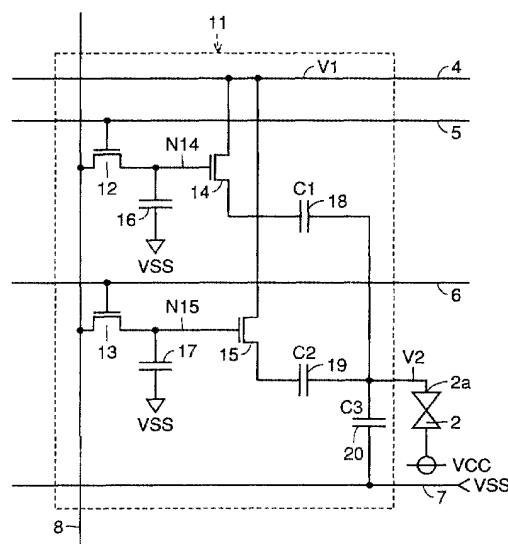
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(54) Liquid crystal display device

(57) In a color liquid crystal display device, two capacitors (18, 19) are both connected in parallel between a pixel signal line (4) and an electrode (2a) of a liquid cell (2), or one of the capacitors is connected therebetween, or none of the capacitors are connected therebetween, in order to selectively set a potential (V2) of the electrode (2a) of the liquid crystal cell (2) in four steps. Therefore, gradation display in four steps can be performed without a digital-to-analog conversion circuit, so that the cost of the device can be reduced.

FIG. 2



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a liquid crystal display device, and in particular to a liquid crystal display device capable of gradation display.

Description of the Background Art

[0002] Conventionally, liquid crystal display devices for displaying static or dynamic image have been utilized in personal computers, television receivers, portable telephones, personal digital assistants, and so forth.

[0003] Fig. 4 is a circuit diagram showing main parts of such a liquid crystal display device. In Fig.4, the liquid crystal display includes a liquid crystal cell 30, a vertical scanning line 31, a common interconnection line 32, a horizontal scanning line 33 and a liquid crystal driving circuit 34, the liquid crystal driving circuit 34 including an N channel MOS transistor 35 and a capacitor 36.

[0004] N channel MOS transistor 35 is connected between horizontal scanning line 33 and one electrode 30a of liquid crystal cell 30, the gate thereof being connected to vertical scanning line 31. Capacitor 36 is connected between electrode 30a of liquid crystal cell 30 and common interconnection line 32. A power-supply potential VCC is applied to the other electrode of liquid crystal cell 30, and a reference potential VSS is applied to common interconnection line 32. Vertical scanning line 31 is driven by a vertical scanning circuit (not shown) and horizontal scanning line 33 is driven by a horizontal scanning circuit (not shown).

[0005] When vertical scanning line 31 is set to a level "H," N channel MOS transistor 35 is conducted, and electrode 30a of liquid crystal cell 30 is charged to the level of horizontal scanning line 33 via N channel MOS transistor 35. For example, the light transmittance of liquid crystal cell 30 will be minimum when electrode 30a is at the level "H," while the light transmittance of liquid crystal cell 30 will be maximum when electrode 30a is at a level "L." A plurality of such liquid crystal cells 30 are arranged in a plurality of rows and columns to form a liquid crystal panel, the panel displaying an image.

[0006] A conventional liquid crystal display device has been configured as described above, so that, in order to perform gradation display in one liquid crystal cell 30, an application of an analog potential corresponding to the gradation was required.

[0007] However, when an image is displayed in response to a digital image signal, a digital-to-analog conversion circuit will be required for converting a digital signal to an analog signal, leading to a problem of higher cost.

SUMMARY OF THE INVENTION

[0008] A main object of the present invention is, therefore, to provide an inexpensive liquid crystal display device capable of gradation display.

[0009] A liquid crystal display device according to the present invention includes a liquid crystal cell receiving a power-supply potential at one electrode thereof and having a light transmittance varied in accordance with a potential applied to the other electrode thereof, a variable capacitance circuit connected between a line of a first reference potential and the other electrode of the liquid crystal cell and having a capacitance value controllable in a plurality of steps, and a control circuit selectively setting the capacitance value of the variable capacitance circuit in response to an image signal to set a potential of the other electrode of the liquid crystal cell. Thus, the light transmittance of the liquid crystal cell can be varied by changing the capacitance value of the variable capacitance circuit, so that gradation display can be performed with one liquid crystal cell without adding a digital-to-analog conversion circuit, and hence the cost of the device will be reduced.

[0010] Preferably, the variable capacitance circuit includes a plurality of first capacitors each having one electrode connected to the other electrode of the liquid crystal cell, and a plurality of first switching elements connected, each at one electrode, to the other electrodes of the plurality of first capacitors, and receiving, each at the other electrode, the first reference voltage. The control circuit renders conductive or non-conductive each of the plurality of first switching elements to selectively set the capacitance value of the variable capacitance circuit. In this case, the light transmittance of the liquid crystal cell can be changed by the number of the first switching elements to be conducted.

[0011] Further, each of the plurality of the first capacitors preferably has a capacitance value different from each other. In this case, gradation display in a larger number of steps will be possible.

[0012] It is also preferable to provide a second capacitor having one electrode connected to the other electrode of the liquid crystal cell, and receiving, at the other electrode, a second reference potential. In this case, more accurate setting of the potential of the other electrode of the liquid crystal cell will be possible.

[0013] More preferably, a plurality of second switching elements connected, each at one electrode, to the other electrodes of the plurality of first capacitors and receiving, each at the other electrode, the second reference potential, and a third switching element having one electrode connected to the other electrode of the liquid crystal cell and receiving, at the other electrode, the second reference potential, are further provided. The control circuit renders conductive the plurality of second switching elements and the third switching element before setting a potential of the other electrode of the liquid crystal cell, to reset the potential of the other electrodes of the plu-

rality of first capacitors and the other electrode of the liquid crystal cell to the second reference potential. In this case, residual charge in the first capacitors and the liquid crystal cell can be removed, so that the potential of the other electrode of the liquid crystal cell can more accurately be set.

[0014] It is also preferable to further provide a fourth switching element having one electrode connected to the other electrode of the plurality of first switching elements, and receiving, at the other electrode, the first reference potential. The control circuit renders non-conductive the fourth switching element after setting a potential of the other electrode of the liquid crystal cell to stop feeding of the first reference potential to the other electrodes of the plurality of first switching elements. This can prevent variation of the other electrode of the liquid crystal cell due to leakage current of the first switching elements.

[0015] More preferably, each of the plurality of first switching elements is a field effect transistor, and a plurality of third capacitors connected, each at one electrode, to respective input electrodes of the plurality of the field effect transistors and receiving, each at the other electrode, a third reference potential, is further provided. The control circuit charges or discharges one electrode of each of the plurality of third capacitors to renders conductive each of the plurality of field effect transistors.

[0016] Further, the liquid crystal display device is preferably installed in a portable electronic device. The present invention will be particularly advantageous in such a case.

[0017] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

Fig. 1 is a block diagram showing a configuration of a color liquid crystal display device according to a first embodiment of the invention;

Fig. 2 is a circuit diagram showing a configuration of a liquid crystal driving circuit included in the color liquid crystal display device shown in Fig. 1;

Fig. 3 is a circuit diagram showing a configuration of a liquid crystal driving circuit in a liquid crystal display device according to a second embodiment of the invention; and

Fig. 4 is a circuit diagram showing a configuration of a liquid crystal driving circuit in a conventional liquid crystal display device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0019] Fig. 1 is a block diagram showing a configuration of a color liquid crystal display device according to a first embodiment of the invention. In Fig. 1, the color liquid crystal display device includes a liquid crystal panel 1, a vertical scanning circuit 9 and a horizontal scanning circuit 10, and is installed, for example, in a portable telephone.

[0020] A liquid crystal panel 1 includes a plurality of liquid crystal cells 2 arranged in a plurality of rows and columns. Liquid crystal panel 1 also includes a pixel signal line 4, a first vertical scanning line 5, a second vertical scanning line 6 and a common interconnection line 7, corresponding to each of the rows, and a horizontal scanning line 8 corresponding to each of the columns.

[0021] Liquid crystal cells 2 are pre-divided into groups for each row, each of the groups including three cells. Three liquid crystal cells 2 in each group are respectively provided with color filters of R, G and B. The three liquid crystal cells 2 in each group form a pixel 3.

[0022] Vertical scanning circuit 9 sequentially selects a row, one by one from the plurality of rows, in response to an image signal, and drives each of pixel signal line 4, the first vertical scanning line 5 and the second vertical scanning line 6 corresponding to each selected row. A reference voltage VSS is applied to common interconnection line 7.

[0023] Horizontal scanning circuit 10 sequentially selects a column, one by one from the plurality of columns, in response to an image signal while vertical scanning circuit 9 is selecting a row, and drives horizontal scanning line 8 corresponding to each selected column.

[0024] When vertical scanning circuit 9 and horizontal scanning circuit 10 have scanned all of liquid crystal cells 2 in liquid crystal panel 1, an image is displayed on liquid crystal panel 1.

[0025] Fig. 2 is a circuit diagram showing a configuration of a liquid crystal driving circuit 11 provided corresponding to each of liquid cells 2. In Fig. 2, liquid crystal driving circuit 11 includes N channel MOS transistors 12-15 and capacitors 16-20, and is connected to a pixel signal line 4, a first vertical scanning line 5, a second vertical scanning line 6 and a common interconnection line 7 in a corresponding row, and to a horizontal scanning line 8 in a corresponding column.

[0026] N channel MOS transistor 14 and capacitor 18 are connected in series between pixel signal line 4 and one electrode 2a of crystal cell 2. N channel MOS transistor 12 is connected between horizontal scanning line 8 and the gate (node N14) of N channel MOS transistor 14, the gate thereof being connected to the first vertical scanning line 5. Capacitor 16 is connected between node N14 and common interconnection line 7.

[0027] N channel MOS transistor 15 and capacitor 19

are connected in series between pixel signal line 4 and one electrode 2a of liquid crystal cell 2. N channel MOS transistor 13 is connected between horizontal scanning line 8 and the gate (node N15) of N channel MOS transistor 15, the gate thereof being connected to the second vertical scanning line 6. Capacitor 17 is connected between node N15 and common interconnection line 7.

[0028] Capacitor 20 is connected between electrode 2a of liquid crystal cell 2 and common interconnection line 7. Power-supply potential VCC is applied to the other electrode of liquid crystal cell 2. The light transmittance of liquid crystal cell 2 varies depending on a voltage between electrodes.

[0029] The operation of this liquid crystal driving circuit 11 is now described. When the first vertical scanning line 5 is set to a level "H," i.e., an activation level, N channel MOS transistor 12 is conducted and node N14 is charged to a level "H" or "L" via horizontal scanning line 8. When the second vertical scanning line 6 is set to the level "H," i.e., the activation level, N channel MOS transistor 13 is conducted and node N15 is charged to a level "H" or "L" via horizontal scanning line 8.

[0030] For example, both nodes N14 and N15 are in the level "H," N channel MOS transistors 14 and 15 are conducted and electrode 2a of liquid crystal cell 2 is connected to pixel signal line 4 via capacitor 18 and N channel MOS transistor 14, and also via capacitor 19 and N channel MOS transistor 15. Assuming here that the potential of pixel signal line 4 is V1, and that the capacitance value of capacitors 18-20 are C1-C3, then a potential V2 of electrode 2a of liquid crystal cell 2 will be $V2 = V1 \times (C1 + C2)/(C1+C2+C3) = Va$.

[0031] If nodes N14 and N15 are in the levels "H" and "L" respectively, N channel MOS transistor 14 is conducted while N channel MOS transistor 15 is non-conducted, and electrode 2a of liquid crystal cell 2 is connected to pixel signal line 4 via capacitor 18 and N channel MOS transistor 14 only. In this case, potential V2 of electrode 2a of liquid crystal cell 2 will be $V2 = V1 \times C1 / (C1 + C3) = Vb$.

[0032] If nodes N14 and N15 are in the levels "L" and "H" respectively, N channel MOS transistor 14 is non-conducted while N channel MOS transistor 15 is conducted, and electrode 2a of liquid crystal cell 2 is connected to pixel signal line 4 via capacitor 19 and N channel MOS transistor 15. In this case, potential V2 of electrode 2a of liquid crystal cell 2 will be $V2 = V1 \times C2/(C2 + C3) = Vc$.

[0033] If both nodes N14 and N15 are in the level "L," N channel MOS transistors 14 and 15 are non-conducted and capacitor 20 will not be charged, and hence, $V2 = 0$.

[0034] Here, if each of C1 and C2 is set to have a value different from each other, it will be possible to selectively set potential V2 of electrode 2a of liquid crystal cell 2 to any one of the potentials in four steps, i.e., Va, Vb, Vc or 0. This enables one liquid crystal cell 2 to perform gradation display in four steps. Therefore, accord-

ing to the first embodiment, the gradation display can be performed without applying an analog potential to pixel signal line 4, and thus the cost of the gradation display can be reduced since no digital-to-analog conversion circuit is required.

[0035] It is noted that capacitor 20 may be dispensed with, since liquid crystal cell 2 have some value of capacitance. In such a case, potential V2 of electrode 2 of liquid crystal cell 2 is determined by potential V1 of pixel signal line 4, capacitance value C1 and C2 of capacitors 18 and 19, and the capacitance value of liquid crystal cell 2.

Second Embodiment

[0036] In liquid crystal driving circuit 11 in Fig. 2, if there is any residual charge in capacitors 18-20, potential V2 of electrode 2a of liquid crystal cell 2 cannot be accurately set to Va, Vb, Vc and 0 described above. The second embodiment is to solve this problem.

[0037] Fig. 3 is a circuit diagram showing main parts of a color liquid crystal display device according to the second embodiment. This is compared with Fig. 2.

[0038] Referring to Fig. 3, this color liquid crystal display device is different from the color liquid crystal display device in the first embodiment, in that a third vertical scanning line 21 and a fourth vertical scanning line 22 are further provided corresponding to each row, so as to replace liquid crystal driving circuit 11 with a liquid crystal driving circuit 23. Liquid crystal driving circuit 23 is different from liquid crystal driving circuit 11 in that N channel MOS transistors 24-27 are added.

[0039] N channel MOS transistor 24 is connected between pixel signal line 4 and N channel MOS transistors 14 and 15, the gate thereof being connected to the third vertical scanning line 21 in a corresponding row. N channel MOS transistor 25 is connected between the source of N channel MOS transistor 14 and common interconnection line 7. N channel MOS transistor 26 is connected between the source of N channel MOS transistor 15 and common interconnection line 7. N channel MOS transistor 27 is connected between electrode 2a of liquid crystal cell 2 and common interconnection line 7. Gates of N channel MOS transistors 25-27 are all connected to the fourth vertical scanning line 22.

[0040] The operation of the color liquid crystal display device is now described. First, the third vertical scanning line 21 and the fourth vertical scanning line 22 are respectively set to levels "L" and "H," and N channel MOS transistor 24 is non-conducted while N channel MOS transistors 25-27 are conducted to allow the residual charge of capacitors 18-20 to be discharged. As a result, one electrode and the other electrode of each of capacitors 18-20 are set to the same potential VSS. It is noted that N channel MOS transistor 24 is non-conducted for the purpose of preventing short-circuit between pixel signal line 4 and common interconnection line 7.

[0041] Subsequently, the third vertical scanning line

21 and the fourth vertical scanning line 22 are set to the levels "H" and "L" respectively, and N channel MOS transistors 25-27 are non-conducted while N channel MOS transistor 24 is conducted. As for the rest, electrode 2a of liquid crystal cell 2 is accurately set to a desired potential, i.e., Va, Vb, Vc or 0 described above, in the same manner as that of the liquid crystal display device in the first embodiment.

[0042] Finally, both the third vertical scanning line 21 and the fourth vertical scanning line 22 are set to the level "L," so that N channel MOS transistors 24-27 are non-conducted. This prevents variation of potential V2 of electrode 2a of liquid crystal cell 2 due to leakage of current from pixel signal line 4 to capacitors 18 and 19.

[0043] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A liquid crystal display device capable of gradation display, comprising:

a liquid crystal cell (2) receiving a power-supply potential (VCC) at one electrode thereof and having a light transmittance varied in accordance with a potential (V2) applied to the other electrode (2a) thereof;

a variable capacitance circuit (14, 15, 18, 19) connected between a line of a first reference potential (V1) and the other electrode (2a) of said liquid crystal cell (2) and having a capacitance value controllable in a plurality of steps; and

a control circuit (9,10) selectively setting the capacitance value of said variable capacitance circuit (14, 15, 18, 19) in response to an image signal to set a potential of the other electrode (2a) of said liquid crystal cell (2).

2. The liquid crystal display device according to claim 1, wherein said variable capacitance circuit (14, 15, 18, 19) includes

a plurality of first capacitors (18, 19) each having one electrode connected to the other electrode (2a) of said liquid crystal cell (2), and a plurality of first switching elements (14, 15) connected, each at one electrode, to the other electrodes of said plurality of first capacitors (18, 19), and receiving, each at the other electrode, said first reference voltage (V1); and said control circuit (9, 10) renders conductive

or non-conductive each of said plurality of first switching elements (14, 15) to selectively set the capacitance value of said variable capacitance circuit (14, 15, 18, 19).

3. The liquid crystal display device according to claim 2, wherein each of said plurality of first capacitors (18, 19) has a capacitance value different from each other.

4. The liquid crystal display device according to claim 2, further comprising:

a second capacitor (20) having one electrode connected to the other electrode (2a) of said liquid crystal cell (2a), and receiving, at the other electrode, a second reference potential (VSS).

5. The liquid crystal display device according to claim 2, further comprising:

a plurality of second switching elements (25, 26) connected, each at one electrode, to the other electrodes of said plurality of first capacitors (18, 19), and receiving, each at the other electrode, the second reference potential (VSS); and

a third switching element (27) having one electrode connected to the other electrode (2a) of said liquid crystal cell (2), and receiving, at the other electrode, said second reference potential (VSS);

said control circuit (9, 10) rendering conductive said plurality of second switching elements (25, 26) and said third switching element (27) before setting a potential (V2) of the other electrode (2a) of said liquid crystal cell (2), to reset the potential (V2) of the other electrodes of said plurality of first capacitors (18, 19) and the other electrode (2a) of said liquid crystal cell (2) to said second reference potential (VSS).

6. The liquid crystal display device according to claim 2, further comprising:

a fourth switching element (24) having one electrode connected to the other electrode of said plurality of first switching elements (14, 15), and receiving, at the other electrode, said first reference potential (V1);

said control circuit (9, 10) rendering non-conductive said fourth switching element (24) after setting a potential (V2) of the other electrode (2a) of said liquid crystal cell (2) to stop feeding of said first reference potential (V1) to the other electrodes of said plurality of first switching elements (14, 15).

7. The liquid crystal display device according to claim

2, wherein

each of said plurality of first switching elements (14, 15) is a field effect transistor, said device further comprising:

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a plurality of third capacitors (16, 17) connected, each at one electrode, to respective input electrodes of said plurality of said field effect transistors (14, 15), and receiving, each at the other electrode, a third reference potential (VSS);

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said control circuit (9, 10) charging or discharging one electrode of each of said plurality of third capacitors (16, 17) to render conductive each of said plurality of field effect transistors (14, 15).

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8. The liquid crystal display device according to claim 1, wherein said liquid crystal display device is installed in a portable electronic device.

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FIG. 1

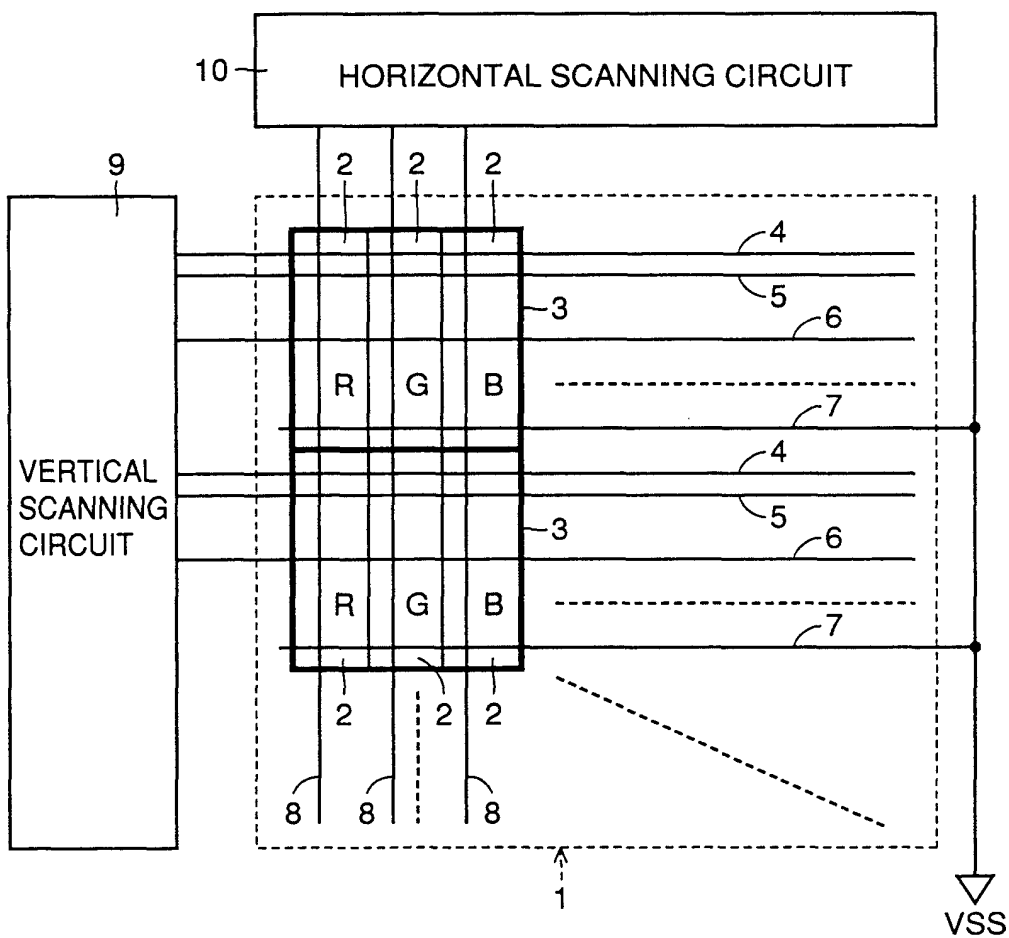


FIG. 2

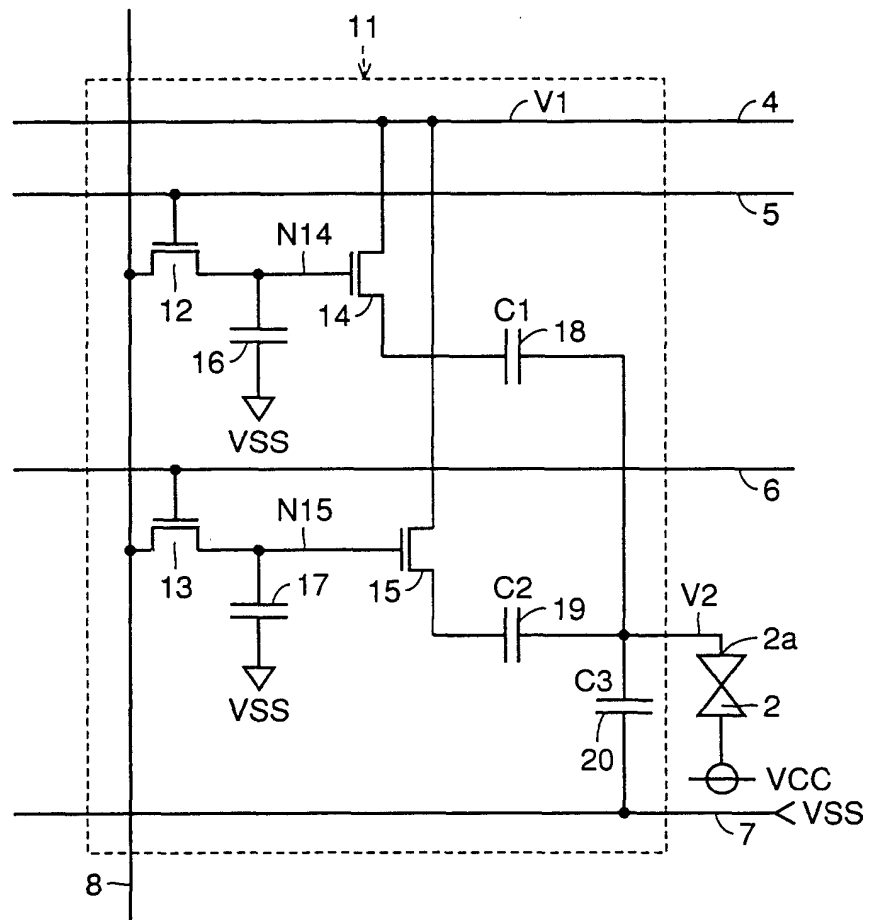


FIG. 3

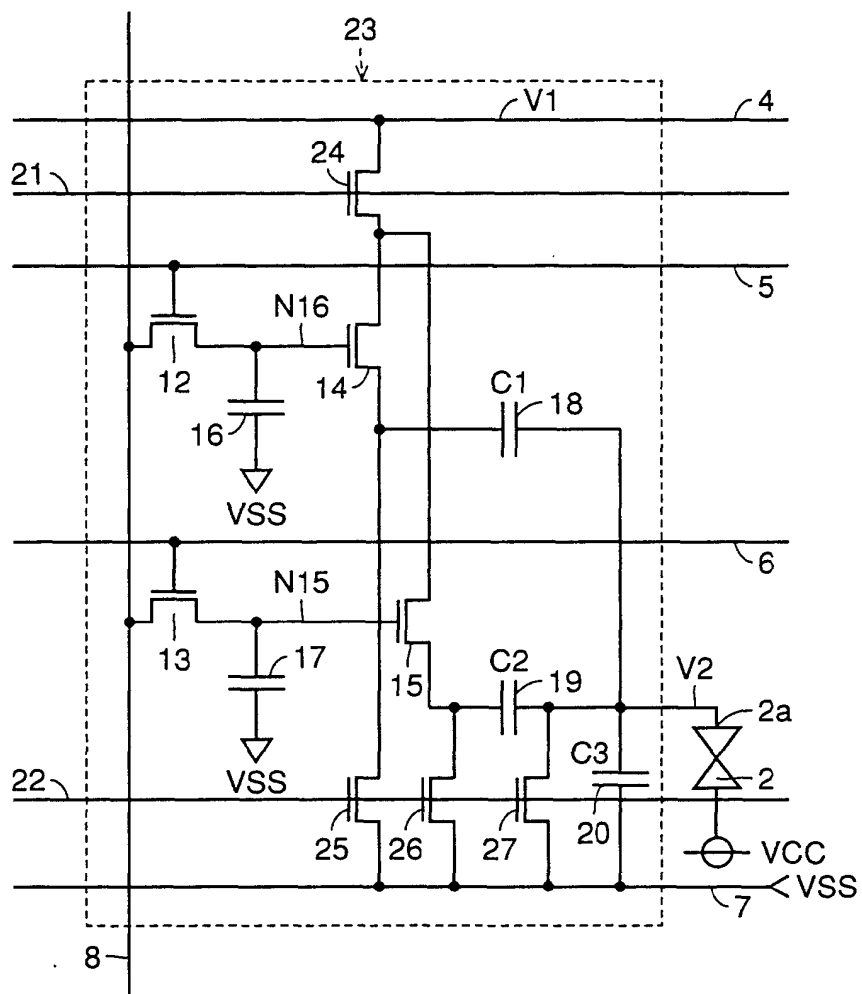
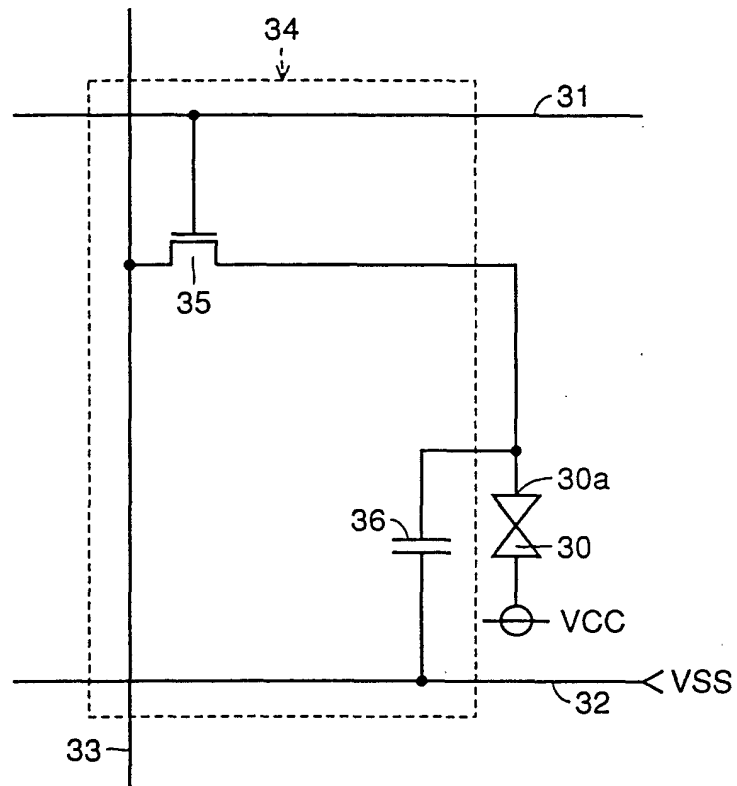


FIG. 4





European Patent
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EUROPEAN SEARCH REPORT

Application Number
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Place of search MUNICH		Date of completion of the search 18 April 2002	Examiner Harke, M
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**ANNEX TO THE EUROPEAN SEARCH REPORT
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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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